Study on voltage regulation method in the power distribution system

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Abstract— This paper focuses on distribution voltage control when over-voltage or under-voltage occurs in the low-voltage (LV) distribution line. The distribution voltage control is performed by transformer and ac-ac converter. Transformer supports a part of settled voltage and ac-ac converter controls voltage disturbance. Bi-directional ac-ac converter employs digital control using Field Programmable Gate Array (FPGA). This method enables simple and fast the distribution voltage control. In this paper, voltage control concept is explained. Scaled-down experimental result is shown, when load condition is changed.

I. INTRODUCTION

In recent years, photovoltaic (PV) systems for grid connection have rapidly spread to solve energy and environmental problem. However, when the clustered PV systems connect with the power distribution system and reverse power flows, there is a possibility that the distribution line voltage increase and exceed the allowable voltage limit. This condition is called over-voltage.

In the present distribution power systems, autotransformer with line drop compensator based step voltage regulator (SVR) have been used. Also, the scheduled operation have controled distribution line voltage in the substation. However, these method are not designed for over-voltage by reverse power flow. Also, the power conditioner of PV is equipped over-voltage relay (OVR). Thus, the electric power from PV systems can not be effectively used.

Therefore, some voltage regulators used power electronics technique have been proposed [1]. Distributed-Unified Power Flow Controller (D-UPFC) is a voltage regulator and able to regulate bi-directional power flow in the distribution systems [2]. D-UPFC consists of transformer and bi-directional ac-ac converter. it can convert directly ac to ac and keep the distribution line voltage to reference voltage. This method enables simple and fast distribution line voltage control.

In this paper, voltage control concept is explained. Scaled-down experimental results are shown, when load condition is changed.

Distribution power system connected clustered PV systems is shown in Fig. 1. When the clustered PV systems connect with distribution system and reverse power flow, the distribution line voltage increase. In this condition, SVR can not control distribution line voltage level. Distribution power system controlled D-UPFC is shown in Fig. 2. D-UPFC controls the voltage to be fixed to reference voltage in allowable voltage window [3].

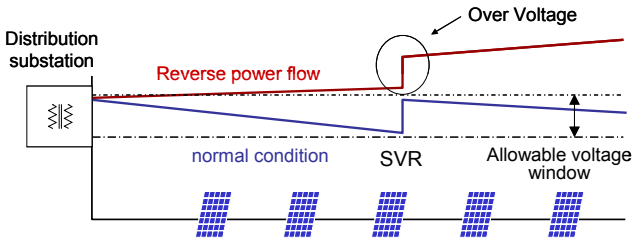


Fig. 1: Distribution power system connected clustered PV systems

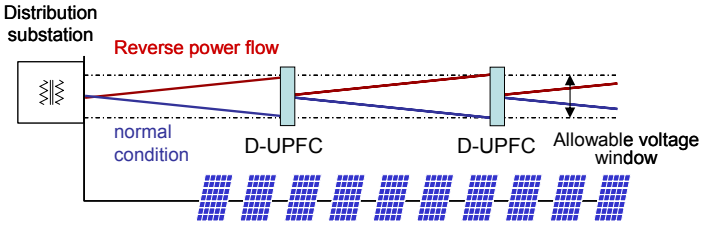


Fig. 2: Distribution power system controlled D-UPFC

II. VOLTAGE CONTROL CONCEPT

A. *Voltage control circuit (D-UPFC)*

Fig. 3 shows the voltage control circuit. V_s is distribution system side voltage and V_{out} is clustered PV systems side voltage. This circuit is installed between distribution the pole transformer primary side and clustered PV systems.

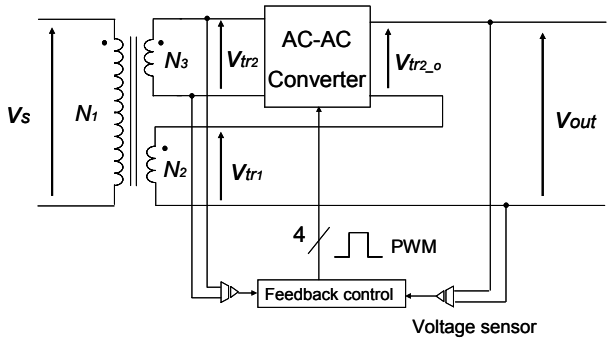


Fig. 3: Voltage control circuit of D-UPFC

Distribution voltage control is performed by transformer and bi-directional ac-ac converter. N_1, N_2, and N_3 are turns

ratio of transformer. Normally N_2 is smaller than N_1 and N_3 is smaller than N_2. V_{tr1} and V_{tr2} are secondary voltage of transformer. Thus, V_{tr1} and V_{tr2} can be expressed,

$$V_{tr1} = \frac{N_2}{N_1} V_s \tag{1}$$

$$V_{tr2} = \frac{N_3}{N_1} V_s \tag{2}$$

V_{tr2_o} is output voltage of bi-directional ac-ac converter. V_{tr2_o} is controlled by pulse width modulation (PWM) signals. PWM signal is made by the feedback control block using Field Programmable Gate Array (FPGA). V_{tr2_o} can be expressed,

$$V_{tr2\_o} = D \times V_{tr2} \tag{3}$$

Where, D is the duty cycle of PWM signal. D-UPFC output voltage V_{out} is decided by V_{tr1} and V_{tr2_o}. V_{out} can be expressed,

$$V_{out} = V_{tr1} + V_{tr2\_o} \tag{4}$$

Therefore, V_{out} can be rewritten as follows

$$V_{out} = \frac{N_2 + (D \times N_3)}{N_1} V_s \tag{5}$$

Thus, transformer supports a part of settled voltage and bi-directional ac-ac converter controls voltage disturbance. If voltage decrease happens in the distribution line, ac-ac converter duty ratio increases. Reversely, when voltage increase occurs in the distribution line, ac-ac converter duty ratio decreases. D-UPFC output voltage V_{out} is kept reference voltage V_{ref}. Vector diagram of D-UPFC voltage control is shown in Fig. 4.

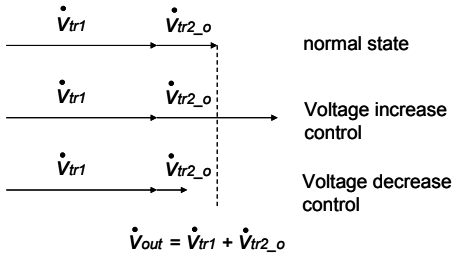


Fig. 4: Vector diagram of D-UPFC voltage control

B. Bi-directional converter

Fig. 5 shows bi-directional ac-ac converter circuit. This converter consists of four MOSFET switches (S_1, S_2, S_3, S_4), input and output filter (L_{in}, C_{int}, L_{out}, C_{out}). This converter is controlled by switching duty as a dc-dc buck converter. So, output voltage is always less than input voltage.

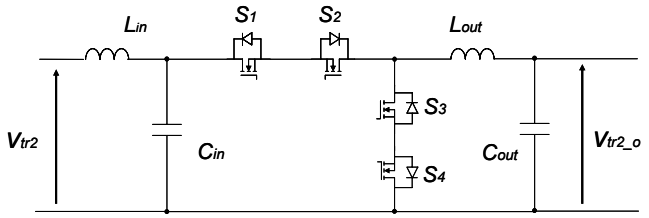


Fig. 5: Bi-directional ac-ac converter circuit

Table 1 shows the switching pattern of ac-ac converter. This switching pattern concept is proposed in referenced paper [4, 5]. Switching pattern is decided by polarity of input voltage V_{tr2}. When V_{tr2} is positive, S_1 and S_3 act PWM signal with 20[kHz]. At the same time, S_2 and S_4 turn on. Reversely, when V_{tr2} is negative, S_2 and S_4 act PWM signal with 20[kHz]. At the same time, S_1 and S_3 turn on all the while. AC-AC converter switching waveform is shown in Fig. 6.

TABLE 1 Switching pattern of the ac-ac converter

$V_{tr2} > 0$	S_1: PWM S_3: $\overline{S_1}$ S_2: ON S_4: ON
$V_{tr2} < 0$	S_1: ON S_3: ON S_2: PWM S_4: $\overline{S_2}$

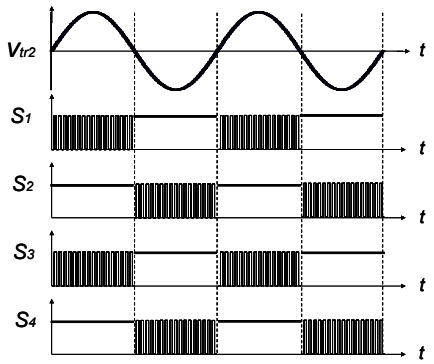


Fig. 6: Switching waveform of ac-ac converter

When the PWM signal changes, there are three operating modes in ac-ac converter [4]. These modes are called active mode, dead time mode, and freewheeling mode. Dead time mode prevents high-voltage spike in the circuit and offers safe commutation. Therefore, the protection circuit such as snubber circuit is not necessary in this converter. Moreover, these modes enable ac-ac converter to control output voltage properly when output current phase is different from output voltage phase by the four quadrant load such as inductive load or capacitive load. So, this ac- ac converter can control the bi-directional power flow in the distribution system. Fig. 7 shows switching waveform of PWM when ac-ac converter input voltage V_{tr2} is positive.

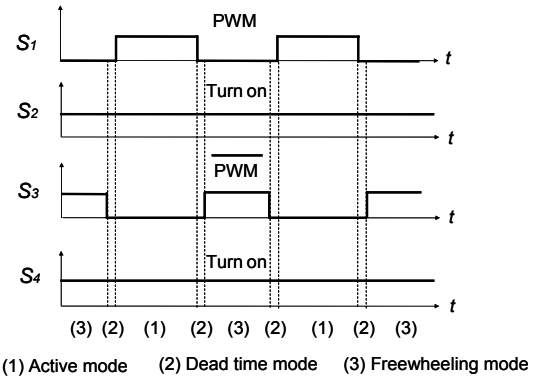


Fig. 7: Switching waveform of PWM signal when ac-ac converter input voltage V_{tr2} is positive

C. *Feedback control block*

D-UPFC employs digital control by field programmable gate array (FPGA). FPGA is integrated circuit (IC) which can rewire an internal circuit by very high speed integrated circuit hardware description language (VHDL). While D-UPFC is controlled, output voltage V_{out} is always kept reference voltage V_{ref}. V_{ref} is decided by distribution line voltage condition.

Fig. 8 shows feed back control block of D-UPFC. V_{out} is detected by voltage sensor. V_{out} changes DC voltage from AC voltage using rms. V_{out_dc} is transformed digital value by analog-digital (A/D) converter and inputted FPGA control block. In the FPGA, error voltage V_{error} is computed and inputted PI compensator. PI compensator gain (K_p, K_i) is depends on D-UPFC control speed and stability. V_{error} is compared triangle waveform V_{tri} with 20[kHz] to make PWM signal V_{pwm}. Finally, V_{pwm} is added dead time and inputted four switches of the ac-ac converter as Table 1.

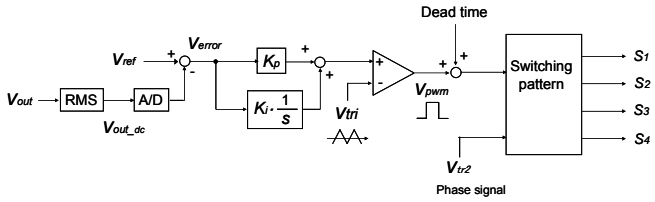


Fig. 8: Feedback control block

III. EXPERIMENTAL DESIGN

Experimental circuits of D-UPFC are shown in Fig. 9. D-UPFC input voltage V_s is supplied 10.0[V,rms]. This voltage is scale down the low-voltage (LV) distribution voltage. And, the transformer turns ratio is

$$N_1 : N_2 : N_3 = 1.0 : 0.9 : 0.2 \qquad (6)$$

Thus, D-UPFC output voltage V_{out} changes from 9.0[V,rms] to 11.0[V,rms]. Also, D-UPFC load has three coditions, normal condition, under-voltage condition, and over-voltage condition. Fig. 10 shows two load conditions. In the normal condition, load is only a resistor (R_{load}). This condition tests D-UPFC fundamental voltage control. In under-voltage condition, shunt resistance (R_{sub}) is connected to R_{load} in parallel by a switch (S_w). This condition simulates that heavy load occurred in the distribution system. R_{sub} is changed in under-voltage condition. Finally, Experimental parameters are shown in table 2.

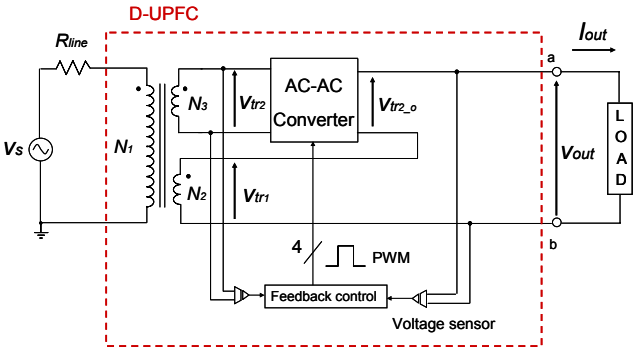


Fig. 9: Experimental circuit of D-UPFC

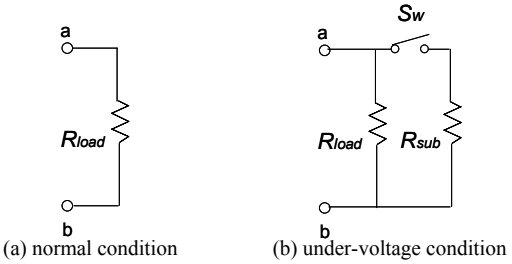


Fig. 10: Experimental conditions of load side.

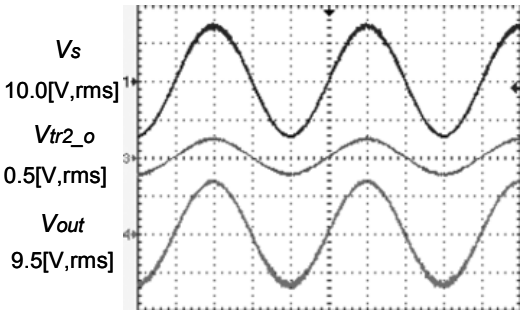
TABLE 2 Experimental parameters

V_s	10.0[V,rms]
N_1:N_2:N_3	1.0:0.9:0.2
L_{in}, L_{out}	2.5[mH]
C_{in}, C_{out}	1.0[uF]
R_{line}	1[Ω]
R_{load}	1[kΩ]
K_p	4.0
K_i	0.25
Circuit frequency	50[Hz]
Switching frequency	20[kHz]

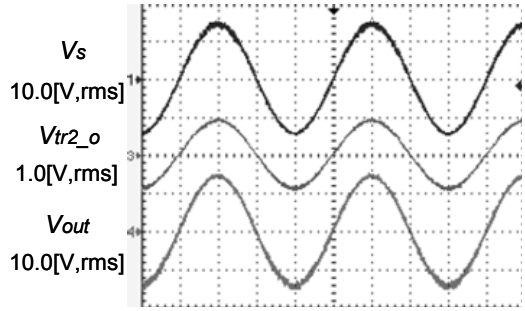
IV. EXPERIMENTAL RESULTS

A. *normal condition*

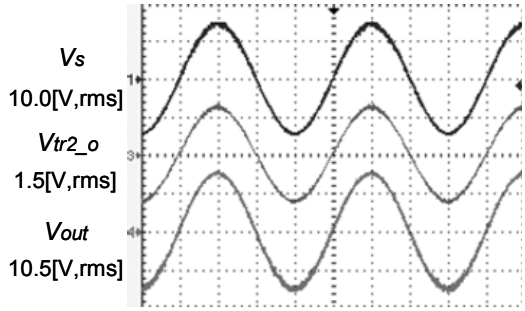
Fig. 11 shows waveform of D-UPFC input voltage V_s, ac-ac converter output voltage V_{tr2_o}, and D-UPFC output voltage V_{out} when reference voltage V_{ref} changed 9.5[V,rms], 10.0[V,rms], and 10.5[V,rms] in FPGA. V_{tr2_o} changed while V_{ref} was changed.



(a) V_{ref} is 9.5[V,rms]



(b) V_{ref} is 10.0[V,rms]



(c) V_{ref} is 10.5[V,rms]

Fig. 11: Waveform of D-UPFC input voltage (V_s), ac-ac converter output voltage (V_{tr2_o}), and D-UPFC output voltage (V_{out}), when the reference voltage (V_{ref}) changed in normal condition. Scales: 10V/div, 10V/div, 2V/div, 10V/div, 10ms/div.

Fig. 12 shows relationship of reference voltage V_{ref} and D-UPFC output voltage V_{out}. V_{out} increases in proportion to V_{ref}.

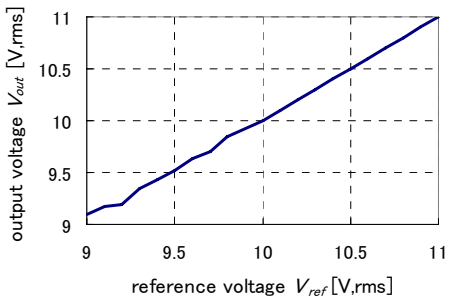


Fig. 12: Relationship of reference voltage (V_{ref}) and D-UPFC output voltage (V_{out}).

Fig. 13 show waveforms of bi-directional ac-ac converter switching pattern. This result is the same switching pattern as table 1. Fig. 14 shows waveform of PWM signal inputted S_1 and S_3, when reference voltage V_{ref} is 10.0[V]. This result shows that duty cycle 0.5 of ac-ac converter. Fig. 15 shows waveform of dead time between S_1 and S_3. In this result, dead time is 250[ns].

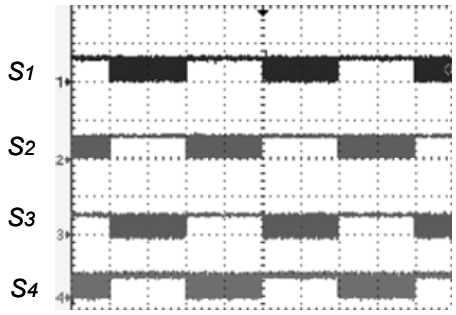


Fig. 13: Switching pattern waveform of switching pattern S_1, S_2, S_3, and S_4, during converter duty cycle 0.5. Scales: 5V/div, 5V/div, 5V/div, 5V/div, 5ms/div

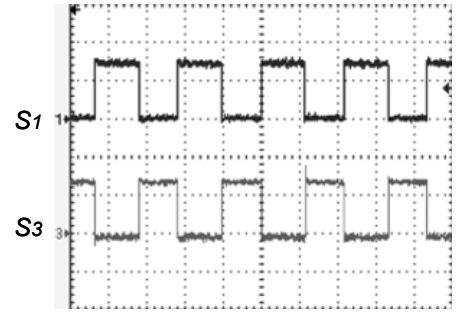


Fig. 14: Switch S_1 and S_3 waveforms during converter duty cycle 0.5. Scales: 2V/div, 2V/div, 25us/div

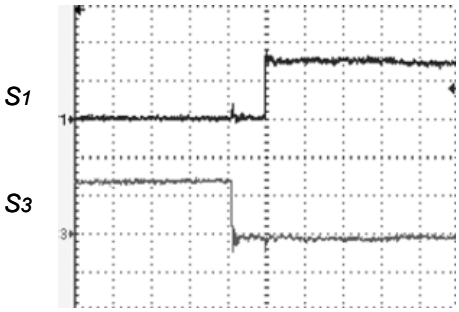


Fig. 15: Dead time waveforms of S_1 and S_3. Scales: 2V/div, 2V/div, 250ns/div.

B. under-voltage condition

Fig. 16 shows relationship of output voltage V_{out} and shunt resistance R_{sub} in under-voltage condition. Additionally, reference voltage V_{ref} was 10.0[V,rms] constant. In under voltage condition, load impedance decreases, at the same time, circuit current increases because R_{sub} is connected to

R_{load} in parallel. When circuit current increases, input voltage drop occurs in the circuit. Therefore, V_{out} decreases due to R_{sub}. When D-UPFC is not connected to the circuit, V_{out} decreases from 10.0[V,rms] to 9.75[V,rms]. However, When D-UPFC is connected to the circuit, V_{out} is constant 10.0[V,rms].

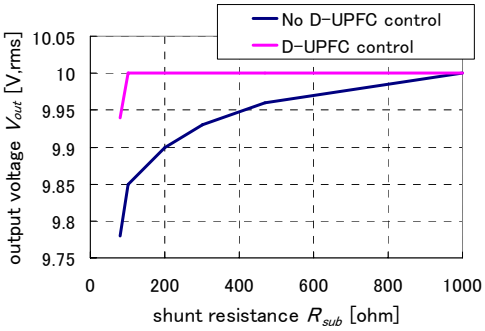


Fig. 16: relationship of reference shunt resistance (R_{sub}) and D-UPFC output voltage (V_{out})

V. CONCLUSION

This paper proposes a distribution voltage regulation method using D-UPFC when over-voltage and under-voltage occurs in the distribution line. Voltage control is performed by transformer and bi-directional ac-ac converter. Experimental results show the D-UPFC fundamental voltage control when load changes from normal condition and under-voltage condition. In the future works, D-UPFC voltage control test is experimented in over-voltage condition.

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