The Development of FPGA-based Digital Controller for PV Inverter

Yusuke Seo[1], Kosuke Kurokawa[1]
[1]Tokyo University of Agriculture and Technology, 2-24-6 Naka-cho, Koganei, Tokyo, 184-8588, Japan,
Phone: +81-42-388-7445, Fax: +81-42-388-7132, E-mail: 50005645118@st. tuat.ac.jp

The development of the FPGA based digital controller for the PV inverter with the typical full-bridge inverter is described. The authors have developed the current control function, the grid connected control function and the MPPT control function using the FPGA. As results of the experiments, the inverter was able to connect the grid in two current control methods. In addition, the MPPT control function was mounted on the FPGA and the stable operation was confirmed. It is presented that the lower control (waveform control etc.) and the higher control (MPPT control) can be controlled by only one FPGA.

Keywords: PV, inverter, digital controller, FPGA

Introduction

According to the Japanese PV2030 roadmap, 100GW cumulative Photovoltaic (PV) installation is expected up to 2030. Japanese domestic market size may be assumed 10 to 20GW/Y [1]. It is necessary that the PV module and the Power conditioner etc. will be mass processed by a production line. In this research, Field Programmable Gate Array (FPGA) which has been mass produced is used as the digital controller for the PV inverters. Now, the current control method for single phase inverter with FPGA has been developed [2], where control responsiveness and high speed calculation of FPGA are shown. However, this control method is not for only the PV inverter. So, the unique control functions for the PV inverter, for example Maximum Power Point Tracking (MPPT) and Islanding detection, have not included.

In this paper, the development of the FPGA based digital controller for the PV inverter with the typical full-bridge inverter is described. The authors have developed and tested the current control function, the grid connected control function and the MPPT control function using the FPGA. The circuit configuration and the experimental results are shown.

Field Programmable Gate Array

FPGA is a logical device that contains a matrix of reconfigurable gate array logic circuitry. Therefore, it is the device which holds the advantages of both, high-speed operation which is feature of the hardware and adaptability which is feature of the software. In addition, FPGA has a function of parallel processing. So, FPGA is possible to utilize in various applications.

Circuit Design within FPGA

As the FPGA controller for the PV inverter, two current control methods are designed. One is the “sensor type” which senses the current reference waveform from the grid voltage waveform. The other is the “data type” which previously stores the current reference waveform data in the FPGA.

Fig.1 shows the block diagram of the constant current control in the “sensor type”. The analog signal of the current reference and the inverter output current converted into digital signal are sent into the FPGA. In the FPGA, the inverter output current is controlled with P control method and the FPGA outputs the PWM signal. The advantage of this method is a high-speed response. The defect is that the distortion of the grid voltage waveform influences the inverter’s output current waveform.

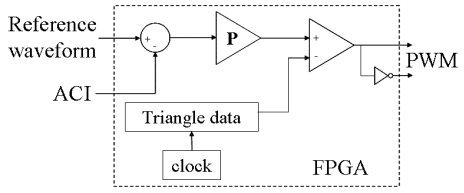

Fig.1.Block diagram of the “sensor type”.

Fig.2 shows the block diagram of the “data type”. Only phase information is extracted from the analog signal of the current reference, the cycle pulse which has the phase information of the grid was input into the FPGA. In synchronous control, the time cycle of the cycle pulse is counted by the counter. The counter outputs the count value which is the frequency information of the cycle pulse. And the frequency of the inverter’s output current is decided by the count value. The digital data is stored in the FPGA for the current reference. After synchronous control, constant current control is applied, and PWM signal is given to the gate-drive IC. The logic of constant current control is the same to the “sensor type”. The advantage of this method is that the inverter can maintain the clean output current waveform. The defect is the response of the output current delays one cycle because the Digital Phase Lock Loop (PLL) uses the frequency of the former period.

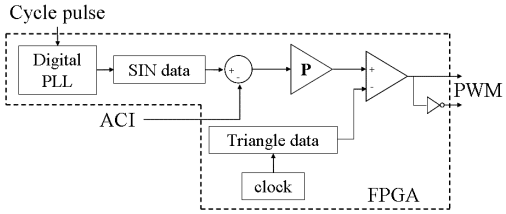

Fig.2.Block diagram of the “data type”.

Fig.3 shows the circuit model. The particular parameters for the system are shown in Table I. The I_d shows the DC current. The i_o shows the inverter’s output current and the i_g shows the current which flows into the R_L(load) from the grid. The ACI, the *ACV*, the *DCI* and the DCV show the signals which are detected from the main circuit. The ACI detects i_o and the *ACV* detects v_g. The *DCI* detects I_d and the *DCV* detects V_d. They are used for the inverter control. The *DCI* and the *DCV* are used for the MPPT.

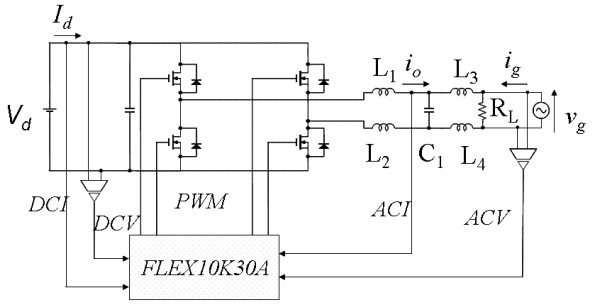

Fig.3.Circuit configuration.

Table 1.Circuit Parameters.

V_d 32V	v_g 40V$_{P\text{-}P}$
L_1, L_2, L_3, L_4 430μH	C_1 4.75μF
R_L 50Ω	Currier frequency 50kHz
FPGA *FLEX10K30A*	MOS-FET *IRF644*
Gate Driver *IR2108*	AD Converter *ADC0820*

Experimental condition

In the experiments of the constant current control, a DC voltage source was used. The current reference waveform was supplied by a function generator. The inverter was not under the grid-connected condition.

In the experiments under the grid connected condition, a DC voltage source was used. The scale-down grid voltage waveform which was a reduced grid voltage waveform with a transformer was used on AC side.

Constant current control

Fig. 4 and Fig. 5 show the observed waveforms of the current reference waveform v_{ref} and the inverter output current waveform i_o in the “sensor type” and the “data type”. In this condition, the AC power source was disconnected. The v_{ref} was supplied by the function generator. From these results, both the “sensor type” and the “data type” operate stably in steady state.

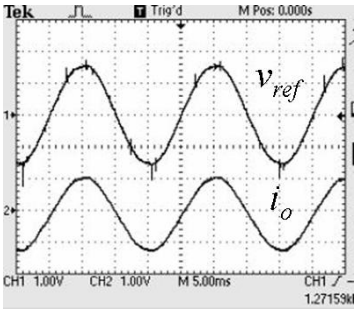

Fig.4.Observed waveforms of v_{ref} and i_o in the “sensor type”. Horizontal: 5ms/div., Vertical: v_{ref}: 1V/div., i_o: 1A/div.

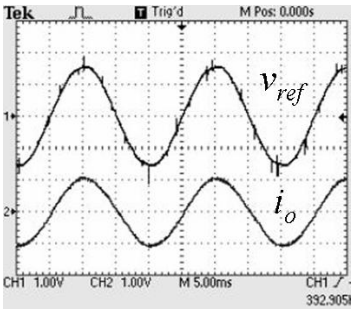

Fig.5.Observed waveforms of v_{ref} and i_o in the “data type”. Horizontal: 5ms/div., Vertical: v_{ref}: 1V/div., i_o: 1A/div.

Fig. 6 and Fig. 7 show the step response of the inverter output waveforms in transient state. Fig 6 shows the result of the “sensor type”. The inverter output the current waveform just as the step input. So it is confirmed that this method is possible to respond to high-speed. Fig 7 shows the result of “data type”. The inverter outputs the current waveform one cycle lately from the step input, because the frequency is counted for the first cycle and the Digital PLL uses the counted value for the next output.

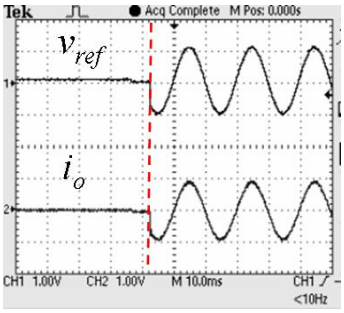

Fig.6.Observed waveforms of v_{ref} and i_o in transient state in the “data type”. Horizontal: 10ms/div., Vertical: v_{ref}: 1V/div., i_o: 1A/div.

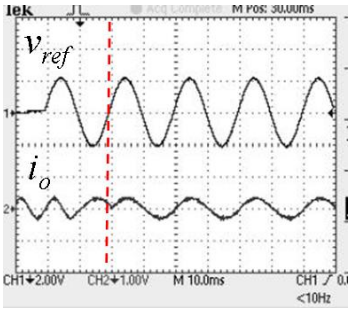

Fig.7.Observed waveforms of v_{ref} and i_o in transient state in the “data type”. Horizontal: 10ms/div., Vertical: v_{ref}: 2V/div., i_o: 1A/div.

Experiments under the grid-connected condition

Fig. 8 and Fig. 9 show the observed waveforms of v_{ref}, i_o and the scale-down grid voltage v_g which is a reduced grid voltage waveform with a transformer. Fig. 8 shows the observed waveforms in the “sensor type” and Fig. 9 shows the result in the “data type”. The i_o synchronized the v_g in both types. This result means that the inverter operates under the grid-connected condition in Power factor 1. It was confirmed that the inverter can output stably in both types.

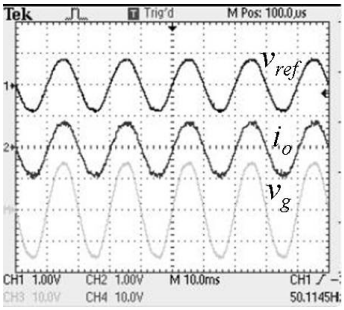

Fig.8.Observed waveforms of v_{ref}, i_o and v_g in the “sensor type”. Horizontal: 10ms/div., Vertical: v_{ref}: 1V/div., i_o: 1A/div., v_g: 10V/div.

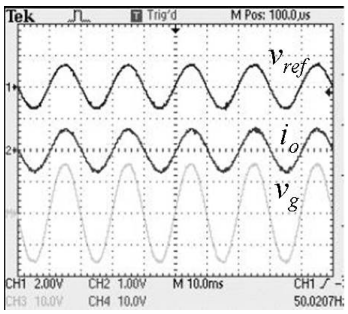

Fig.9.Observed waveforms of v_{ref}, i_o and v_g in the “data type”. Horizontal: 10ms/div., Vertical: v_{ref}: 1V/div., i_o: 1A/div., v_g: 10V/div.

Fig. 10 and Fig. 11 show the results of analysis of the output current distortion under the grid-connected condition. Fig. 10 shows the result in the “sensor type”. The 9th and 11th harmonics were more than 3%, and the Total Harmonics Distortion (THD) was 6.01%. In this cause, the influence of the transformer characteristic which was used is considered. THD of the scale-down grid voltage waveform was 1.97%. On the other hand, Fig. 11 is the result of the “data type”. In this case, the harmonics of each degree were less than 3%, and The THD was 3.49%. The As the results, the “data type” satisfied the stipulation of the technical guide in Japan [3].

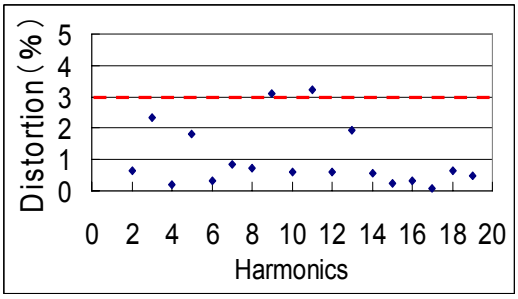

Fig.10. Distortion of output current in the “sensor type”.

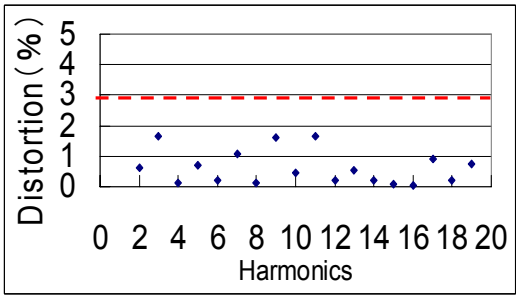

Fig.11. Distortion of output current in the “data type”.

MPPT control using the FPGA

System configuration

The system was configured from a ready-made FPGA board, main board, AD converter board and voltage sensor board. The cement register (50Ω40W) was used as load. Instead of a PV module, a DC voltage source was used. In addition, the potentiometer was connected in series, so the I-V curve of PV was simulated. The bipolar power source which can operate in four quadrants was used on AC side.

MPPT control logic

Various MPPT control logics have been developed, in this paper, authors used the method that adjusting the

parameter k changes the i_o, therefore V_d and I_d are controlled by adjusting the parameter k [4]. The output of the MPPT loop is the parameter k that can control the output the inverter's output current. The inverter's output i_o is given by the following equation (1):

$$i_o = i_{o\_MAX} \times k \qquad (1)$$

where i_o shows the value of the inverter output current, i_{o_MAX} shows the value of rated current, and $k\,(0 \le k \le 1)$ shows the parameter of the inverter operation.

To decide the maximum power point, the P&O method [5] is used. Fig 12 shows the block diagram in the FPGA. The high-speed loop (constant current control and PWM control) was configured by the"data type". In the FPGA, this high-speed loop and the MPPT loop was designed in parallel. The MPPT loop outputs the parameter k, and the high-speed loop receives this value. Therefore, the inverter changes control its power toward the MPP.

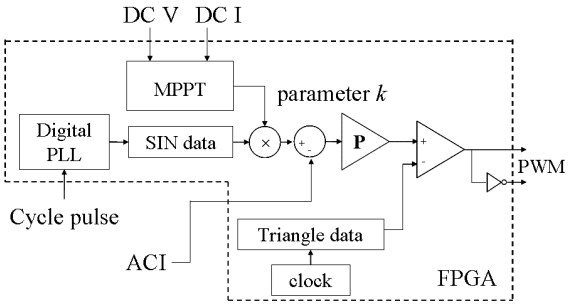

Fig.12. Block diagram of the FPGA mounting the MPPT.

Experimental results of MPPT function

Fig. 13 shows the observed waveforms. The DC current waveform I_d and the inverter's output current waveform i_o increase gradually, and the DC voltage waveform V_d decreases. On the other hand, the grid voltage waveform v_g is constant. The waveforms show that the inverter increases its output power, so the MPPT control operates normally. Additionally, the AC current waveform i_g increases. The reverse current from the inverter flows into the grid in this condition, so the phase of the i_o is in reverse compared to the v_g.

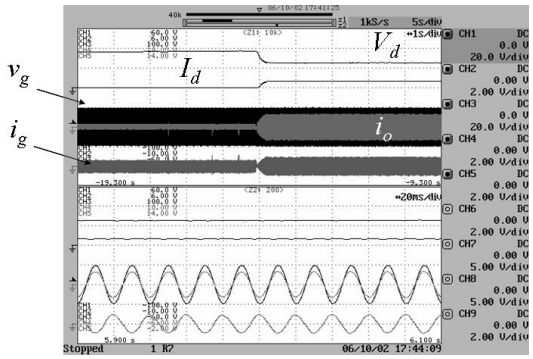

Fig.13. Observed waveforms of V_d, I_d, v_g, i_o and i_g in the MPPT operation. Horizontal: (up): 1s/div., (down): 20ms/div., Vertical: V_d: 20v/div., I_d: 2A/div., v_g: 20v/div., i_o: 2A/div., i_g: 2A/div.

Conclusion

This paper has presented a prototype of the digital controller based on FPGA for PV inverter. The experiments were carried out utilizing FLEX10K30A FPGA (ALTERA Corp.). The "sensor type" and the "data type" have been developed, and the inverter is able to be connected to the grid in both types. In addition, the MPPT control function is mounted on the FPGA and the stable operation has been confirmed. The lower control (waveform control etc.) and the higher control (MPPT control) are realized by only the FPGA.

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